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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,805	TAMURA ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *8 and 9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6 and 7* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 02/03/04, 09/14/04, 11/22/04, 01/04/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 are presented for examination.

2. The IDS filed on 02/03/2004, 09/14/2004, 11/22/2004 and 01/04/2005 have been received and carefully considered.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-7, drawn to construction of a storage system and method for controlling it, classified in class 711, subclass 117.

II. Claims 8 and 9, drawn to a method for verifying an alternating path structure in a memory control device, classified in class 708, subclass 164.

4. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as verifying an alternating path structure in a memory control device without using the invention I. See MPEP § 806.05(d).

5. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

6. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

7. During a telephone conversation with Attorney, Carl Brundidge (Reg. No.: 29,621), on 03/15/2006 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-7. Affirmation of this election must be made by applicant in replying to this Office action. Claims 8 and 9 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

8. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Specification

9. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

10. The abstract of the disclosure is objected to because the abstract as submitted in this application is *not* limited to a single paragraph. Correction is required. See MPEP § 608.01(b).

Drawings

11. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the intermediate memory hierarchy constructed as disclosed in claim 3 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

12. Claim 1 is objected to because of the following informalities:

It is unclear that whether the term "a memory device" in line 11 refers to "at least one or more memory devices" in line 8 or a "new" memory device other than "at least one or more memory devices" in line 8.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 1-3 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

14. Claim 1 recites the limitation "this logical unit" in line 8. There is insufficient antecedent basis for this limitation in the claim. It is unclear whether the term "this logical unit" in line 8 refers to "at least one or more logical units" in lines 5-6 or a "new" logical unit other than "at least one or more logical units" in lines 5-6.

15. Similarly, claim 2 recites the limitation "the memory device " in line 11; claim 3 recites "said memory device", "this first memory hierarchy", "the memory device" and "said first memory hierarchy" in it; and claim 5 recites "said memory device" in it. There is insufficient antecedent basis for these limitations in these claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

16. Claims 1-2 and 6-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Voigt et al. (USPN: 6,684,313) hereinafter, Voigt.

As per claim 1, Voigt teaches a storage system (shown in Fig. 8) constructed by communicably connecting a first storage controller (i.e. 54a in Fig. 8) and a second storage controller (i.e. 54b in Fig. 8) and performing data processing according to a request from a host device (i.e. 22 in Fig. 8), wherein said first storage controller coupled to at least one or more logical units (i.e. logical group 0-3, 110, 120 and 130 in Fig. 1) accessed by said host device, and at least one or more intermediate memory hierarchies (i.e. 62a in Fig. 8) arranged so as to connect this logical unit and at least one or more memory devices, and at least one of said intermediate memory hierarchies

(i.e. 62b in Fig. 8) is connected to a memory device (i.e. 52 in Fig. 8) arranged in said second storage controller (i.e. 54b in Fig. 8). Although, Voigt teaches that the first storage controller has at least one or more intermediate memory hierarchies, i.e. at least one or more intermediate memory hierarchies (i.e. 62a in Fig. 8) are within the first storage controller (i.e. 54a in Fig. 8), Voigt does not clearly teach that the first storage controller has at least one or more logical units, i.e. Voigt does not clearly teach that at least one or more logical units are within the first storage controller. However, since the logical unit is not a physical entity, it has to be a part of the control circuitry (i.e. 54a in Fig. 8) (e.g. see Col. 9, lines 26-67 and Figs. 1 and 8).

As per claim 2, Voigt teaches a memory control device (i.e. 54a in Fig. 8) communicably connected to a host device (i.e. 22 in Fig. 8) and a second storage controller (i.e. 54b in Fig. 8) and performing data processing according to a request from said host device, and coupled to: at least one or more logical units (i.e. logical group 0-3, 110, 120 and 130 in Fig. 1) accessed by said host device; and at least one or more intermediate memory hierarchies (i.e. 62a in Fig. 8) arranged so as to connect said logical unit and at least one or more memory devices; wherein at least one of said intermediate memory hierarchies is connected to the memory device arranged in said second storage controller (i.e. 54b in Fig. 8). Although, Voigt teaches that the first storage controller has at least one or more intermediate memory hierarchies, i.e. at least one or more intermediate memory hierarchies (i.e. 62a in Fig. 8) are within the first storage controller (i.e. 54a in Fig. 8), Voigt does not clearly teach that the first storage controller has at least one or more logical units, i.e. Voigt does not clearly teach that at

least one or more logical units are within the first storage controller. However, since the logical unit is not a physical entity, it has to be a part of the control circuitry (i.e. 54a in Fig. 8) (e.g. see Col. 9, lines 26-67 and Figs. 1 and 8).

As per claim 6, Voigt teaches a control method of a memory control device (i.e. 54a in Fig. 8) communicably connected to a host device (i.e. 22 in Fig. 8) and a second storage controller (i.e. 54b in Fig. 8) and performing data processing according to a request from said host device, and including: a step for obtaining path information to a memory device (i.e. 52 in Fig. 8) arranged in said second storage controller; and a step for mapping said obtained path information to an intermediate memory hierarchy (i.e. 62 a in Fig. 8) connected to a logical unit (i.e. one of logical group 0-3, 110, 120 and 130 in Fig. 1) accessed by said host device (e.g. see Figs. 1 and 8 and Col. 9, lines 26+).

As per claim 7, Voigt teaches a computer program for setting a memory device (i.e. 52 in Fig. 8) arranged in a second storage controller (i.e. 54b in Fig. 8) to a memory control device (i.e. 54a in Fig. 8) as an internal volume, and making the computer execute: a step for obtaining path information to a memory device (i.e. 52 in Fig. 8) arranged in said second storage controller; and a step for mapping said obtained path information to an intermediate memory hierarchy (i.e. 62 a in Fig. 8) connected to a logical unit (i.e. one of logical group 0-3, 110, 120 and 130 in Fig. 1) accessed by said host device (e.g. see Figs. 1 and 8 and Col. 9, lines 26+).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Voigt in view of Chai et al. (USPN: 5,504,882) hereinafter, Chai.

As per claim 3, Voigt teaches the claimed invention as described above, but failed to teach the further limitation of how the intermediate memory hierarchy is constructed. Chai, however, teaches that the intermediate memory hierarchy (i.e. the cache 22 in 14 and 40 of Fig. 3) is constructed by arranging at least one or more first memory hierarchies set (i.e. the cache 22 in the first group of storage controllers 14 in Fig. 3) on said memory device, and at least one or more second memory hierarchies set (i.e. the cache 22 in the second group of storage controllers 40 in Fig. 3) on this first memory hierarchy, and the memory device arranged in said second storage controller is mapped to said first memory hierarchy (e.g. see Fig. 3). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of current invention was made to construct the intermediate memory hierarchy as taught by Chai. In doing so, it provides the high degree of reliability of disk array systems by utilizing a controller device that is split into a first level and second level controller. The first and second level controllers are interconnected in a manner such that a failure of the second level controller associated with a first level controller will result in a switching of a peer

controller into the path utilized by the faulting second level controller. Therefore, it is being advantageous.

As per claim 4, Voigt teaches the claimed invention as described above. However, Voigt does not teach that the memory control device further comprises plural logical units able to be accessed from said host device through plural paths different from each other, and each of said logical units is connected to each of said intermediate memory hierarchies. Chai, on the other hand, teaches that the memory control device further comprises plural logical units (i.e. 44 in Fig. 3) able to be accessed from said host device (i.e. 10 in Fig. 3) through plural paths (i.e. different paths as shown in Fig. 3) different from each other, and each of said logical units is connected to each of said intermediate memory hierarchies (i.e. the cache 22 in 14 and 40 of Fig. 3) (e.g. see Fig. 3). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of current invention was made to implement Chai's teachings in the memory control device taught by Voigt. In doing so, it provides the high degree of reliability of disk array systems by utilizing a controller device that is split into a first level and second level controller. The first and second level controllers are interconnected in a manner such that a failure of the second level controller associated with a first level controller will result in a switching of a peer controller into the path utilized by the faulting second level controller. Therefore, it is being advantageous.

Allowable Subject Matter

18. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MATTHEW KIM
SUPERVISORY PATENT EXAMINER